UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/581,111	05/31/2006	Hubert Moriceau	291619US0PCT	5366

22850 7590 03/03/2008

OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
NIKMANESH, SEAHVOSH J	

ART UNIT	PAPER NUMBER
2812	

NOTIFICATION DATE	DELIVERY MODE
03/03/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@oblon.com
oblonpat@oblon.com
jgardner@oblon.com

Office Action Summary	Application No.	Applicant(s)	
	10/581,111	MORICEAU ET AL.	
	Examiner	Art Unit	
	SEAHVOSH J. NIKMANESH	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-20* is/are rejected.

7)☒ Claim(s) *1-9 and 14-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *5/31/2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/14/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is in response to the information disclosure statement filed 8/14/2006.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

3. It is suggested that the claim to priority be made at the beginning of the specification.

Information Disclosure Statement

4. The information disclosure statement filed 8/14/2006 has been considered. Please note the correction to reference AA, since the document number has been corrected to the following: 2003/0211705.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 1 recites the limitation "the coating" in line 3. There is insufficient antecedent basis for this limitation in the claim, claims 2-9 and 14-17 depend on claim 1.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-6, 8-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Tong et al., US PGPub 2003/0211705 A1.

a. **Regarding claim 1**, Tong et al. shows a method for molecular adhesion of a second electronic compound (44/45) on a first electronic compound (40/41), the contact surface of the first electronic compound containing a polymer [0053] comprising the coating [0054], with a bonding layer (46) at least some of the surface of the polymer contained at the surface of the first electronic compound, with the molecular adhesion taking place between said bonding layer and the second electronic compound (Figs. 4A-4E; [0054]-[0058]).

b. **Regarding claim 2**, Tong et al. shows the cleaning of the contact surface of the second electronic compound and/or its coating with a layer similar to the bonding layer (Figs. 4A-4E; [0043] and [0054]).

c. **Regarding claim 3**, Tong et al. shows that the thinning of the second electronic compound after adhesion thereof to the bonding layer ([0061]; i.e. lapping, polishing,

etching, etc.).

d. **Regarding claim 4**, Ting et al. shows the heat treatment of the assembly of the two compounds after adhesion ([0060]; i.e. annealing the bonded wafers).

e. **Regarding claim 5**, Tong et al. shows that the coating is produced by deposition of a bonding layer having a thickness between 50 and 300 nm ([0088]; i.e. the oxide thickness of 0.3μm formed by PECVD).

f. **Regarding claim 6**, Tong et al. shows the polishing of the bonding layer and/or its activation (Fig. 3b; [0044]).

g. **Regarding claim 8**, Tong et al. shows the cross-linking of the polymer prior to the coating thereof ([0049]-[0057]; i.e. the surface is subjected to VSE and/or RIE to terminate the surface with desired gas to form the bonding interface and then brought together to bond the wafers).

h. **Regarding claim 9**, Tong et al. shows that the bonding layer consists of silicon oxide [0054].

j. **Regarding claim 10,** Tong et al. shows Claim 10: Method for producing an array of stacked electronic compounds comprising the development of at least one first electronic compound so that the surface of the first electronic compound at least partially consists of a polymer ([0041] and [0053]-[0054]; Figs. 4A-4E).

k. **Regarding claim 11,** Tong et al. shows the three-dimensional array of electronic compounds comprising a plurality of interface layers, wherein each of the interface layers is at least equal to the surface of the array at the level of said interface layer, so that at least some of the interface layers directly separate a polymer from at least one electronic component (Figs. 4A-4E; [0054]-[0060]; Example 1).

l. **Regarding claim 12,** Tong et al. shows a stack of electronic compounds, wherein each compound has the same shape and/or size as the adjacent compound from which it is separated by an interface layer (Figs. 4A-4E; [0054]-[0060]; Example 1).

m. **Regarding claim 13,** Tong et al., shows that the interface layers consist of silicon oxide, silicon nitride and/or silicon oxynitride [0054].

n. **Regarding claim 14:** Method according to claim 1, wherein the coating is produced by deposition of a bonding layer made of silicon oxide having a thickness between 50 and 300 nm ([0088]; i.e. the oxide thickness of 0.3μm formed by PECVD).

o. **Regarding claim 15**, Tong et al., shows the polishing and/or the activation of the silicon layer (Fig. 3b; [0044]).

p. **Regarding claim 16,** Tong et al., shows the cross-linking of the polymer prior to the coating thereof ([0049]-[0057]; i.e. the surface is subjected to VSE and/or RIE to terminate the surface with desired gas to form the bonding interface and then brought

together to bond the wafers).

q. **Regarding claim 17,** Tong et al., shows a method for producing an array of stacked electronic compounds comprising the development of at least one first electronic compound so that the surface of the first electronic compound at least partially consists of a polymer ([0041] and [0053]-[0054]; Figs. 4A-4E).

r. **Regarding claim 18,** Tong et al. shows a method for molecular adhesion of a second electronic compound on a first electronic compound, the contact surface of the first electronic compound containing a polymer ([0041] and [0053]-[0054]; Figs. 4A-4E), comprising the cross-linking of the polymer ([0049]-[0057]; i.e. the surface is subjected to VSE and/or RIE to terminate the surface with desired gas to form the bonding interface and then brought together to bond the wafers), the coating with silicon oxide, silicon nitride and/or silicon oxynitride [0054], of at least some of the surface of the polymer contained at the surface of the first electronic compound, the polishing and/or activation of said silicon layer [0044], with the molecular adhesion taking place between said silicon layer and the second electronic compound ([0054]-[0057]).

s. **Regarding claim 19,** Tong et al., shows the heat treatment of the assembly of the two compounds after adhesion ([0060]; i.e. annealing the bonded wafers).

t. **Regarding claim 20,** Tong et al., shows the thinning of the second electronic

compound after adhesion thereof ([0061]; i.e. lapping, polishing, etching, etc.).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SEAHVOSH J. NIKMANESH whose telephone number is (571)270-1805. The examiner can normally be reached on Mon through Fri 7:30 -5:00 E.S.T.. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Seahvosh J Nikmanesh/
Examiner, Art Unit 2812
/Scott B. Geyer/
Primary Examiner, Art Unit 2812